CLAIMS

[1] A semiconductor device package structure comprising:

a semiconductor chip mounted interposer configured by mounting a semiconductor chip to an interposer in which inside terminals to which terminals of a semiconductor chip to be mounted are connected, outside terminals to which terminals other than the terminals of the semiconductor chip are connected, and conductive wiring that makes an electrical connection between the outside terminals and the inside terminals are formed, and

a substrate-like or frame-like base material on which a plurality of semiconductor chips are mounted, wherein

the semiconductor chip mounted interposer is mounted along with another semiconductor chip to the base material, and the semiconductor chip mounted interposer and the other semiconductor chip are resin sealed along with the base material.

[2] The semiconductor device package structure according to claim 1, wherein the semiconductor chip mounted interposer is mounted on a semiconductor chip that is mounted to the base material.

[3] The semiconductor device package structure according to claim 1, wherein a plurality of the semiconductor chip mounted interposer are provided, and those semiconductor chip mounted interposers are disposed laminated on the base material.

[4] The semiconductor device package structure according to

claim 1, wherein the semiconductor chip mounted interposer is configured by mounting semiconductor chips to both faces of the interposer, sandwiching the interposer.

[5] The semiconductor device package structure according to claim 1, wherein the semiconductor chip mounted interposer is configured by disposing a plurality of semiconductor chips laminated on the interposer.

[6] The semiconductor device package structure according to claim 1, wherein the semiconductor chip mounted interposer is configured by resin sealing the semiconductor chip mounted on the interposer along with the interposer, separate from resin sealing to the base material.

[7] The semiconductor device package structure according to claim 1, wherein the interposer, in a state before being mounted to the base material, is provided with terminals for connecting to a testing apparatus in order to perform predetermined reliability testing or operation testing, and the semiconductor chip mounted interposer, in a state before being mounted to the base material, has been subjected to the predetermined reliability testing or operation testing using the terminals.

[8] A semiconductor device packaging method comprising configuring a semiconductor chip mounted interposer by mounting a semiconductor chip to an interposer in which inside terminals to which terminals of a semiconductor chip to be mounted are

connected, outside terminals to which terminals other than the terminals of the semiconductor chip are connected, and conductive wiring that makes an electrical connection between the outside terminals and the inside terminals, are formed; mounting the semiconductor chip mounted interposer to a substrate-like or frame-like base material; and resin sealing the semiconductor chip mounted interposer together along with the base material.

[9] The semiconductor device packaging method according to claim 8, wherein in a state before the interposer is mounted to the base material, terminals for connecting a testing apparatus are provided in the interposer, predetermined reliability testing or operation testing is performed by connecting the testing apparatus to the terminals, and after performing the reliability testing or operation testing the terminals are detached and the semiconductor chip mounted interposer is configured, and the semiconductor chip mounted interposer is mounted to the base material.